SAG Element 23.1 : Moving head disc C.U.
Baseline 3 : Element Design Specifications

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Element 23.1 : Moving Head Disc Control Unit

Baseline 3 : Element Design Specifications

TYPE OF PAGE : SURVEY OF DOCUMENTS

SECTION OR TYPE OF PAGE											SIGNATURE			First issue = O Changed = X Cancelled = V Not applicable = N	
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9 - SPECIAL CIRCUITS

CONTENTS

I - GENERAL

1.1. Description

The special circuits for Moving Head disc control unit x 1210 include

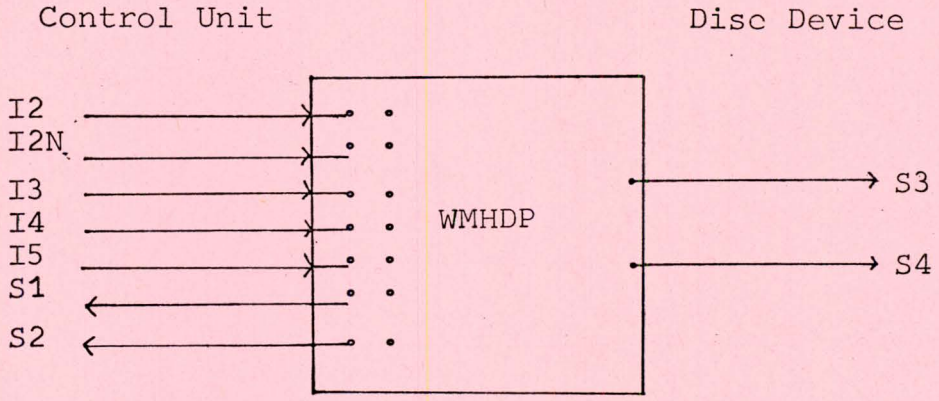
- a write circuit
- a read circuit
- interface circuits, i. e. 10 input adaptors and 22 output adaptors for two disc unit connection.

1.2. Performance specification

See Sag. EPS - Bas. 2 - El. 23.1

2 - C.A.D. Data

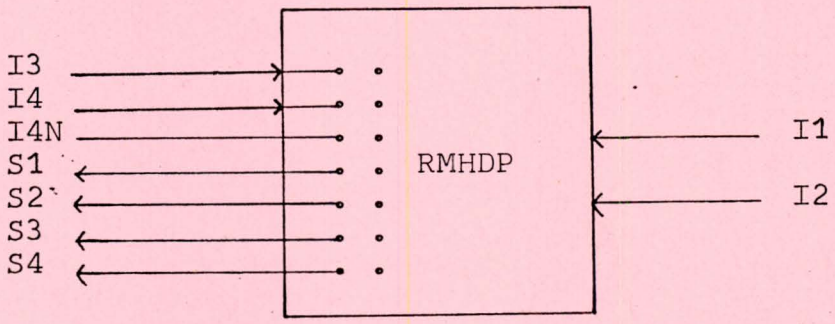
2.1. Write circuit



Only one WMHDP circuit is used per control unit .. means that this circuit is isolated from logic part.

INPUTS			OUTPUTS		
CAD Name.	Logic Name.	Fan-in	CAD Name.	Logic Name.	Fan-out
I2	SELA	1	S1	WDP	30
I2N	SELAN	1	S2	WCP	30
I3	DATAO	1	S3	WØO	
I4	WGATE	1	S4	WØ1	
I5	CPINH	1			

2.2. Read circuit



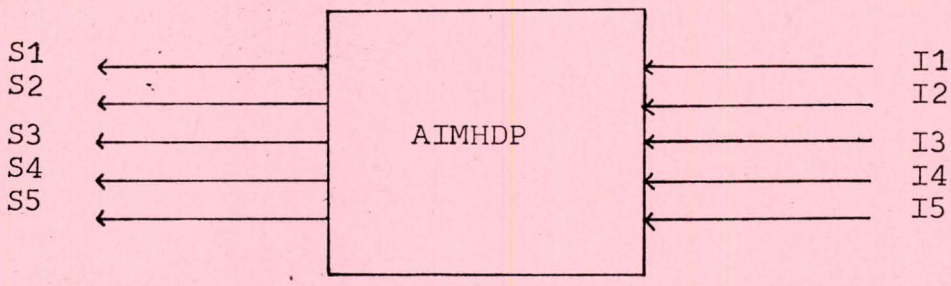
Only one RMHDP circuit is used per control unit

. . means that this circuit is isolated from logic part.

INPUTS			OUTPUTS		
CAD Name.	Logic Name.	Fan-in	CAD Name.	Logic Name.	Fan-out
I1	RDLO		S1	RDP	10
I2	RDLI		S2	RCP	10
I3	RGATE	2	S3	DATAI	10
I4	SELA	1	S4	MP	10
I4N	SELAN	1			

2.3. Interface circuits

2.3.1. Input adaptors

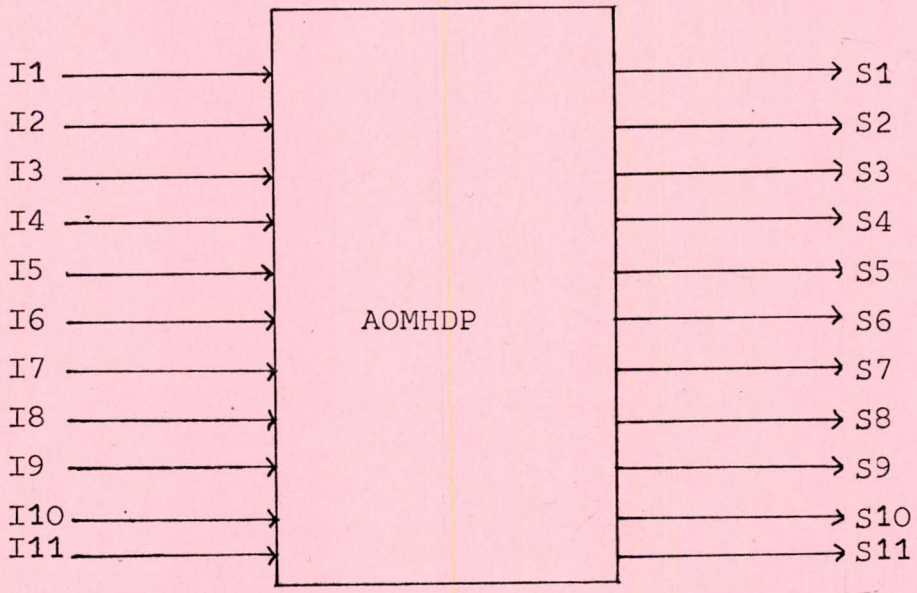


There exist two circuits identical to this one, when two disc units are needed.

INPUTS			OUTPUTS		
CAD Name	Logic Name.	Fan-in	CAD Name.	Logic Name.	Fan-out
I2	SSN i		S1	SPi	10
I2	ISN i		S2	IPi	10
I3	URN i		S3	RDIi	10
I4	OCN i		S4	ONCYLi	10
I5	UUN i		S5	UNSAFi	10

$i = \begin{cases} 1 \\ 2 \text{ only when two disc units are needed} \end{cases}$

2.3.2. Output adaptors



There exist two circuits identical to this one, when two disc units are needed.

INPUTS			OUTPUTS		
CAD Name.	Logic Name.	Fan-in	CAD Name.	Logic Name.	Fan-out
I1	CBO	1	S1	CON B OiN	
I2	CB1	1	S2	CON B 1iN	
I3	CB2	1	S3	CON B 2iN	
I4	CB3	1	S4	CON B 3iN	
I5	CB4	1	S5	CON B 4iN	
I6	CB5	1	S6	CON B 5iN	
I7	CB6	1	S7	CON B 6iN	
I8	CB7	1	S8	CON B 7iN	
I9	TAGCONTi	1	S9	TCSiN	
I10	TAGHEADi	1	S10	TMSiN	
I11	TAGDIFi	1	S11	TDSiN	

$$i = \begin{cases} 1 \\ 2 \text{ only when two disc units are needed} \end{cases}$$

3 - DIAGRAM AND COMPONENTS

3.1. Write circuit

3.1.1. Diagram

See next page.

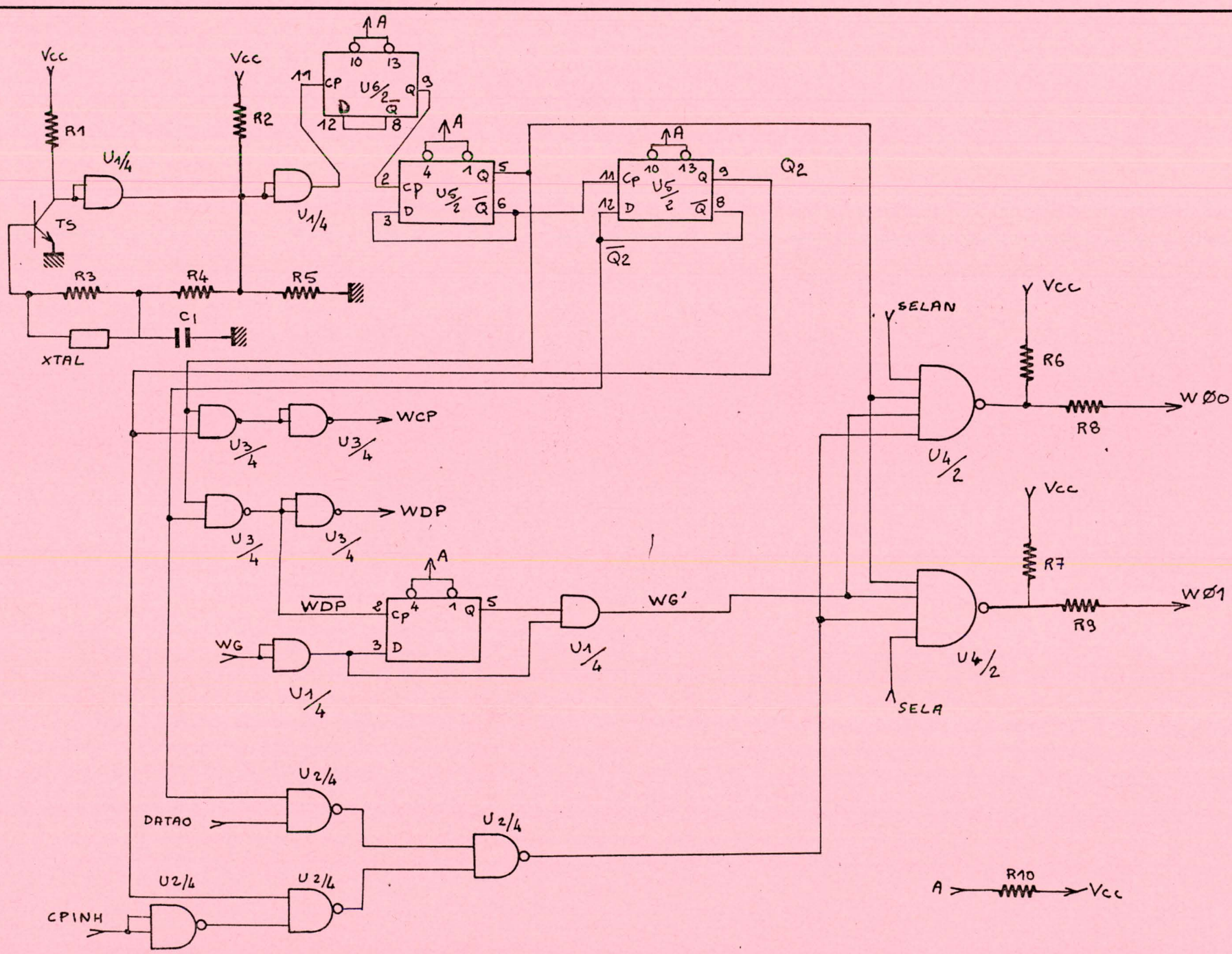
3.1.2. Components

R1, R3	3,16 KΩ	1/8W	Metal film resistor
R2	464Ω	1/8W	" "
R4	2,15 KΩ	1/8W	" "
R5	681Ω	1/8W	" "
R6, R7	270Ω	1/8W	" "
R8, R9	39Ω	1/8W	" "
R10	1 KΩ	1/8W	" "
U1	U6A 7408 59X		
U2	U6A 7400 59X		
U3	U6A 7437 59X		
U4	U6A 7440 59X		
U5	U6A 74H74 59X		
U6	U6A 7474 59X		
TS	2N 2369		
C1	1nf miniature ceramic plate - class. 2		
XTAL	6,66 MHZ QACR 19		

1 socket for quartz HC 6/U

Each IC is decoupled by a ceramic plate capacitor 3,3 nf.

i. e. : 6 capacitors for write circuit



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ELEMENT 23.1 : MOVING HEAD DISC CONTROL UNIT
BASELINE 3 : ELEMENT DESIGN SPECIFICATIONS
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3.2. Read circuit

3.2.1. Diagram

See next page.

3.2.2. Components

R1, R2	330 Ω	1/8W	Metal film resistor
R3, R4	31,6KΩ	1/8W	" "
R5, R7	2,16KΩ	1/8W	" "
R6	3,16KΩ	1/8W	" "
R8	1 KΩ	1/8W	" "
GR1, GR2	BAX 13		

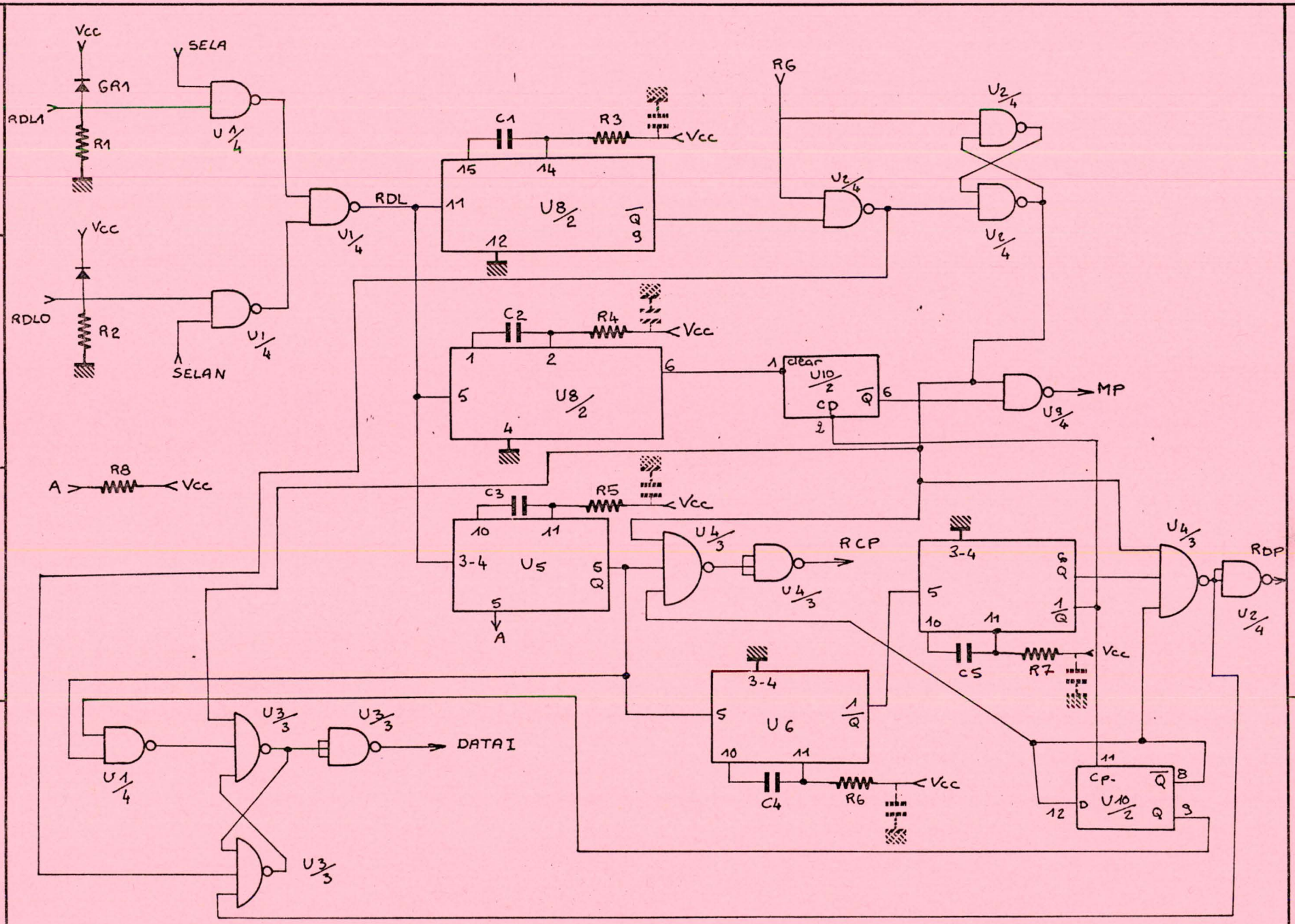
C1	56 pf	Miniature ceramic plate
C2	120 pf	class 1 B (NPO)
C3, C5	68 pf	
C4	82 pf	

U1, U2	U6A 7400 59X
U3, U4	U6A 7410 59X
U8	U7B 9602 59X
U5, U6, U7	SN 74121J
U9	U6A 7408 59X
U10	U6A 7474 59X

All IC's are decoupled by a ceramic plate capacitor 3,3 nf.

i. e. : 10 capacitors for Read circuit

Note that, for U5, U6, U7, U8, each capacitor must be put close to resistor end connected to Vcc, as shown in dotted lines.



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ELEMENT 23.1 MOVING HEAD DISC CONTROL UNIT
BASELINE 3 : ELEMENT DESIGN SPECIFICATIONS
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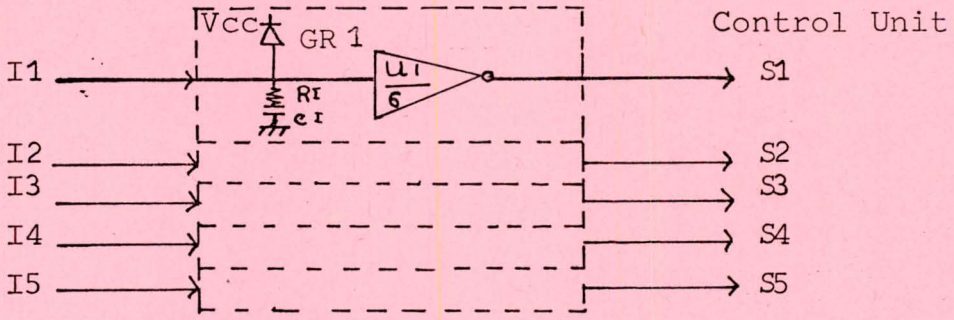
3.3. Interface circuits

3.3.1. Input adaptors

3.3.1.1. Diagram



3.3.1.2. Components for one Disc Unit Interface

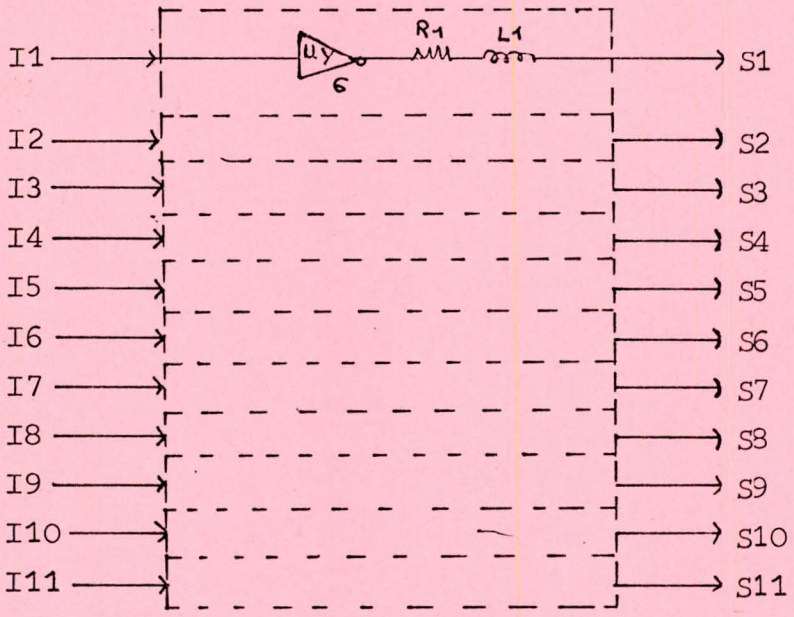
R1 - R5	5 x 178Ω	1/8W	Metal film resistor
C1 - C5	5 x 825pf		ceramic plate
GR1-GR5	5 x BAX 13		
U1	U6A 740459X		

This IC is decoupled by a ceramic plate capacitor 3,3nF.

i. e. 1 capacitor for one disc unit interface.

3.3.2. Output adaptors

3.3.2.1. Diagram



3.3.2.2. Components for one Disc Unit Interface

R1 - R11	11 x 68,1Ω	1/8W	Metal film resistor
L1 - L11	11 x 10 µH		
2 x U1	U6A 7404 59X		

Each IC is decoupled by a ceramic plate capacitor 3,3 nF.

i. e. 2 capacitors for one Disc Unit interface

4 - FUNCTIONAL SPECIFICATIONS

4.1. Write circuit

The high frequency clock (3,33 MHZ) made with XTAL and U1, drives the asynchronous counter U6, the second part of which selects the pulses either towards WDp or towards WCp at the output of WØO or WØ1, which depends on SELA state ; appears the wave depending on CPINH, DATAO, and WG states, as required in SAG. El. 23.1. B. 2. With U3, and U7, the first negative pulse which appears on WØO (or 1) is synchronous with WCp, by means of WG'.

4.2. Read circuit

RDL is provided either by RDL1 or by RDLO, depending on SELA state.

U5, U6, U7 are one shot non rettrigerable monostables of typical pulse width respectively 110ns, 200ns, 110ns.

U5 and U7 are for RCp and RDp. U6 is for a delay between RCp and RDp. The second part of U10 Flip-flop clocked by U7 . $\overline{Q}$ is for providing RCp and RDp, only when C pulse on RDL appears.

U8 is a dual rettrigerable monostable. The first parts of U8, and U10 determine MP (typical pulse width for this monostable 1400 ns).

The second part of U8 (typical pulse width 750ns) is for first hole detection in RDL, when RG.

U8 and U5 are trailing edge triggered

U6 and U7 are leading edge triggered

4.3. Interface circuits

Input and output adaptors are for interface between Control Unit and Disc Unit. Both are inverting the signal.

5 - ELECTRICAL SPECIFICATIONS

5.1. Write circuit

5.1.1. Power Supply

Vcc = 5V ± 5 %

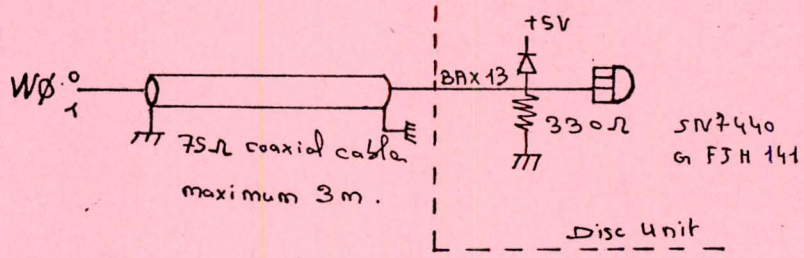
Icc = 146 mA typ.

230 mA max.

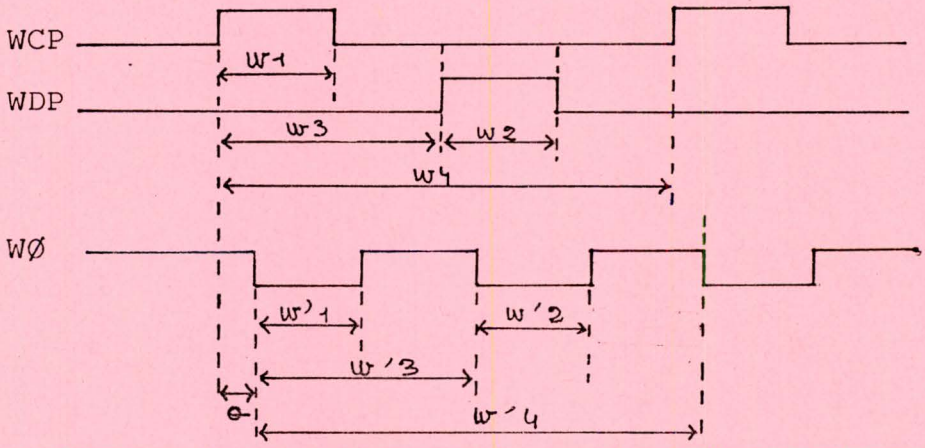
5.1.2. Input and Output voltages

VL ≤ 0,4 V VH ≥ 2,4 V

When used, WØO or WØ1, are loaded as follows



5.1.3. Waveforms



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5.2. Read circuit

5.2.1. Power Supply

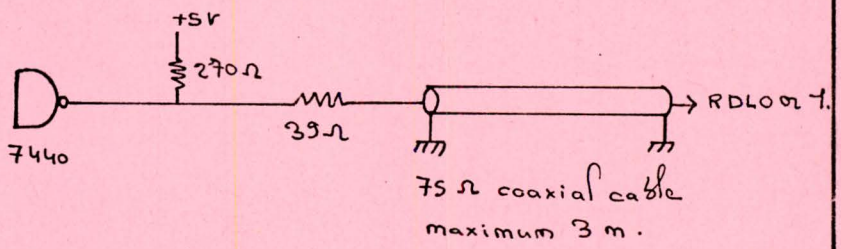
Vcc = 5V ± 5 %

Icc = 190 mA typ.
320 mA max.

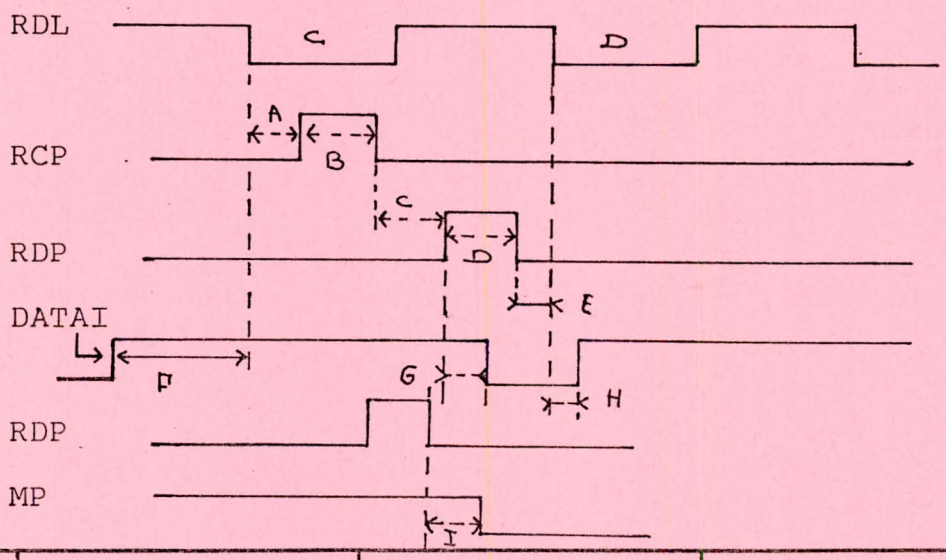
5.2.2. Input and Output voltages

VL ⩽ 0,4 V VH ⩾ 2,4 V

RDLO (or RDL1) is provided by the following circuit



5.2.3. Waveforms



5.3. Interface circuits

5.3.1. Input adaptors

5.3.1.1. Power Supply

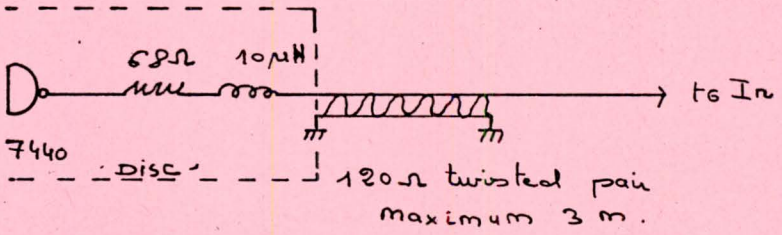
Vcc = 5 V ± 5 %

Icc = 12 mA typ.
23 mA max. — For one Disc device

24 mA typ.
45 mA max. — For two Disc devices

5.3.1.2. Special loading rules

In (n=1,..,5) is provided by the following circuit.



5.3.2. Output adaptors

5.3.2.1. Power Supply

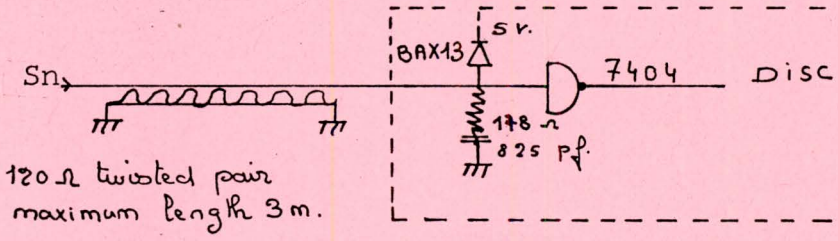
Vcc = 5 V ± 5 %

Icc = 24 mA typ.
45 mA max. — For one Disc device

48 mA typ.
90 mA max. — For two Disc devices

5.3.2.2. Special loading rules

Sn (n = 1,...,11) is loaded as follows



6 - MEASUREMENTS

6.1. Write circuit

6.1.1. Results

Measurements at circuit outputs with no charge (except probe one)

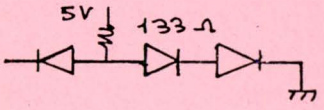
- Influence of temperature (Vcc = 5V)

Parameter \ T°C	0°	25°	70°
W1 (W'1)	315 ns	311 ns	317 ns
W2 (W'2)	315 ns	313 ns	315 ns
W3	609 ns	602 ns	599 ns
W'3	600,5ns	600,5ns	600,5ns
W4 (W'4)	1201,00 ns	1201,01 ns	1201,03 ns
θ	3 ns	5 ns	- 3 ns

- Influence of Vcc variations ± 5 % 25°C

none. (probe loading)

- Influence of Fan-out Vcc = 5 V 25°C

Fan-out	Probe	Max allowed	Note
W1	311 ns	316 ns	F.O = 30 simulated by 
W2	313 ns	312 ns	
W3	602 ns	606 ns	
W4	1201,01 ns	1201,01 ns	
θ	5 ns	4 ns	

Vcc	5V - 5 %	5V	5V + 5 %
Icc	120 mA	123 mA	140 mA

All rise and fall times are $\leqslant$ 20 ns.

6.1.2. Summary

Parameter	Required	Typically measured	Worst - case
W1 (W'1)	300ns ± 60ns	311ns	285ns$\leqslant$W1$\leqslant$330ns
W2 (W'2)	300ns ± 60ns	313ns	285ns$\leqslant$W2$\leqslant$330ns
W3	600ns ± 30ns	602ns	600ns ± 19ns
W'3	600ns*	600ns	600ns ± 1ns
W4 (W'4)	1200ns*	1201ns	1200ns ± 2ns
θ	-50ns$\leqslant$0$\leqslant$50ns	5ns	- 34ns$\leqslant$θ$\leqslant$ 9ns

Note : worst-case includes IC's variations.

* ± 1% pulse to pulse variations ± 0,3% long terme stability.

6.2. Read circuit

6.2.1. Results

Measurements at circuit outputs with no charge (except probe one)

- Influence of temperature and Vcc

in ns.

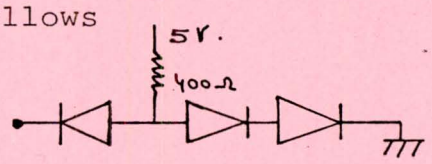
1st line Vcc = 5,25 V
2nd line Vcc = 5 V
3rd line Vcc = 4,75 V

T°	0°	25°	70°
A	49,5 51 53	49,5 51 52	50 51 53
B	112 110 109	108 108 107	112 111 111
C	163 168 170	158 160 162	161 164 168
D	116 116 114	112 111 112	114 114 112
E	151 149 148	158 156 152	145 144 140

F	540 540 540	510 510 510	520 518 516
G	10 10 9	9,5 9,5 9	10,5 10 10
H	68 72 75	55 60,5 50	71 73,5 75
I	22 23 23	15 14,5 14,5	16 16 16,5

- Influence of Fan-out

Each value of previous table (for probe load) must be increased by 2ns maximum for a 10 fan-out simulated as follows



Vcc	4,75 V	5 V	5,25 V
Icc	132 mA	140 mA	152 mA

All rise and fall times are $\leq$ 20 ns.

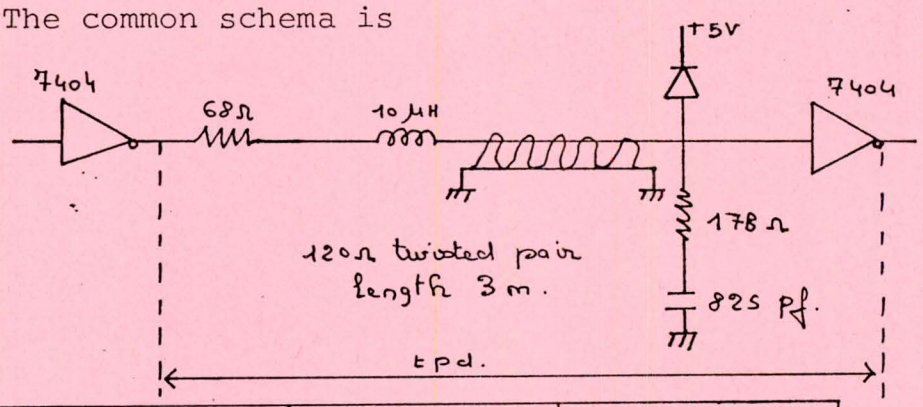
6.2.3. Summary

Parameter	Required	Typically measured	Worst case
A	$\leqslant$ 110ns	51ns	31ns $\leqslant$ A $\leqslant$ 107ns
B	110ns $\pm$ 10ns	108ns	110ns $\pm$ 6ns
C	$\geqslant$ 100ns	160ns	106ns $\leqslant$ C $\leqslant$ 277ns
D	110ns $\pm$ 10ns	111ns	110ns $\pm$ 6ns
E	$\geqslant$ 0	156ns	$\geqslant$ 15ns
F	$\geqslant$ 100ns	510ns	188ns $\leqslant$ F $\leqslant$ 776ns
G	$\leqslant$ 40ns	9,5ns	-16ns $\leqslant \theta \leqslant$ 34ns
H	$\geqslant$ 30ns	60,5ns	37ns $\leqslant \theta \leqslant$ 144ns
I	$\leqslant$ 100ns	14,5ns	$\leqslant$ 71ns

Note : Worst case includes IC's variations.

6.3. Interface circuits

The common schema is



	Required	Measured	Expected
tpd +	120 ns typ 150 ns max	103 ns	150 ns
tpd -	90 ns typ 120 ns max	78 ns	120 ns